NEC

MOS FIELD EFFECT TRANSISTOR

NP84N075CUE, NP84N075DUE, NP84N075EUE

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance

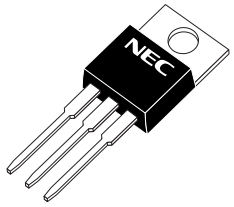
★ $R_{DS(on)}$ = 12.5 mΩ MAX. (V_{GS} = 10 V, I_D = 42 A)

★ • Low C_{iss} : C_{iss} = 5600 pF TYP.

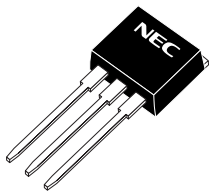
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP84N075CUE	TO-220AB
NP84N075DUE	TO-262
NP84N075EUE	TO-263

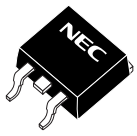
(TO-220AB)



(TO-262)



(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

	Drain to Source Voltage	V_{DSS}	75	V
	Gate to Source Voltage	V_{GSS}	±20	V
	Drain Current (DC) Note1	$I_{D(DC)}$	±84	A
★	Drain Current (Pulse) Note2	$I_{D(pulse)}$	±260	A
	Total Power Dissipation (T_A = 25°C)	P_T	1.8	W
	Total Power Dissipation (T_C = 25°C)	P_T	200	W
★	Single Avalanche Current Note3	I_{AS}	19 / 52 / 73	A
★	Single Avalanche Energy Note3	E_{AS}	333 / 250 / 50	mJ
	Channel Temperature	T_{ch}	175	°C
	Storage Temperature	T_{stg}	–55 to +175	°C

★ **Notes 1.** Calculated constant current according to MAX. allowable channel temperature.

2. PW ≤ 10 μs, Duty cycle ≤ 1 %

3. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{GS} = 20 V→0 V

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	0.75	°C/W
Channel to Ambient	$R_{th(ch-A)}$	83.3	°C/W

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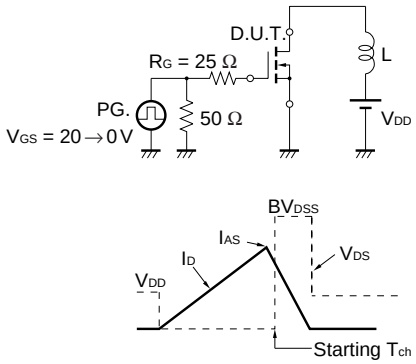
The mark ★ shows major revised points.

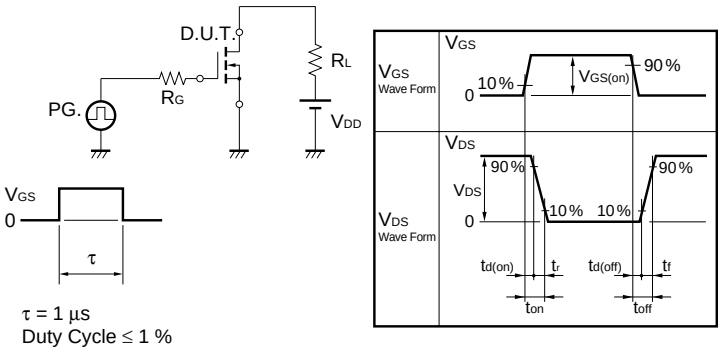
★ ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 42 A		9.3	12.5	mΩ
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 42 A	21	43		S
Drain Leakage Current	I_{DSS}	V_{DS} = 75 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		5600	8400	pF
Output Capacitance	C_{oss}			530	800	pF
Reverse Transfer Capacitance	C_{rss}			270	490	pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 42 A, $V_{GS(on)}$ = 10 V, V_{DD} = 38 V,		30	66	ns
Rise Time	t_r	R_G = 0 Ω		15	38	ns
Turn-off Delay Time	$t_{d(off)}$			72	150	ns
Fall Time	t_f			12	30	ns
Total Gate Charge	Q_G	I_D = 84 A, V_{DD} = 60 V, V_{GS} = 10 V		100	150	nC
Gate to Source Charge	Q_{GS}			24		nC
Gate to Drain Charge	Q_{GD}			35		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 84 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 84 A, V_{GS} = 0 V, di/dt = 100 A/μs		70		ns
Reverse Recovery Charge	Q_{rr}			200		nC

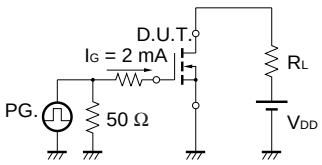
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

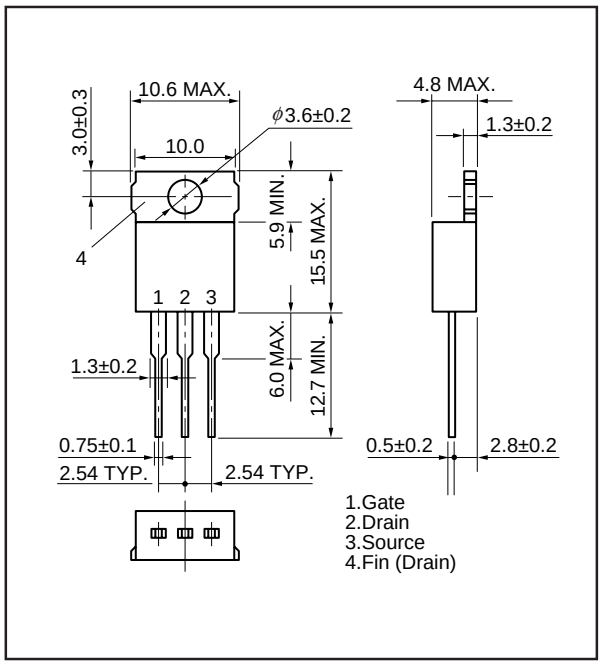


TEST CIRCUIT 3 GATE CHARGE

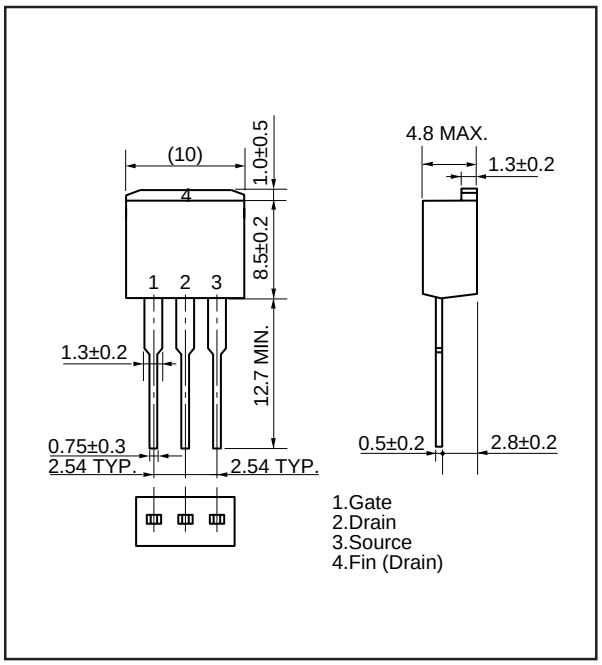


PACKAGE DRAWINGS (Unit: mm)

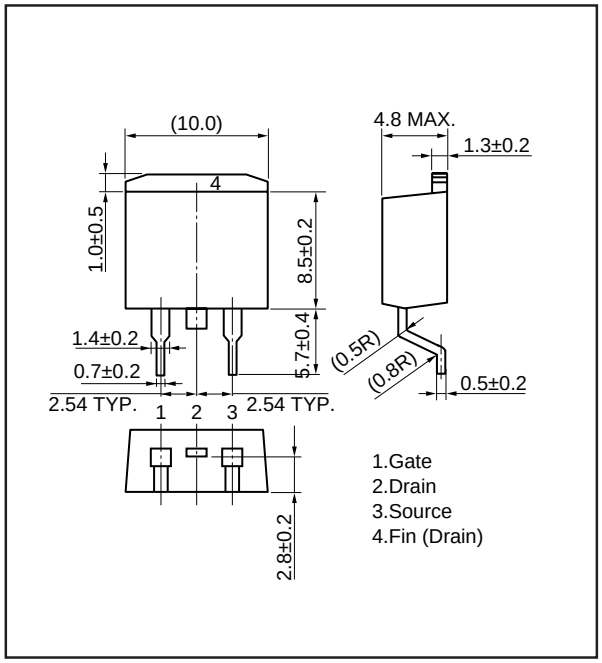
1) TO-220AB (MP-25)



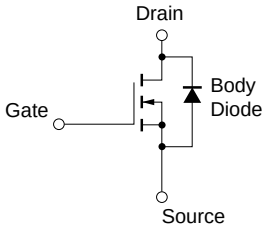
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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